Combined FEOL/BEOL Process Sweet Spot Search for Chip Performance Optimization

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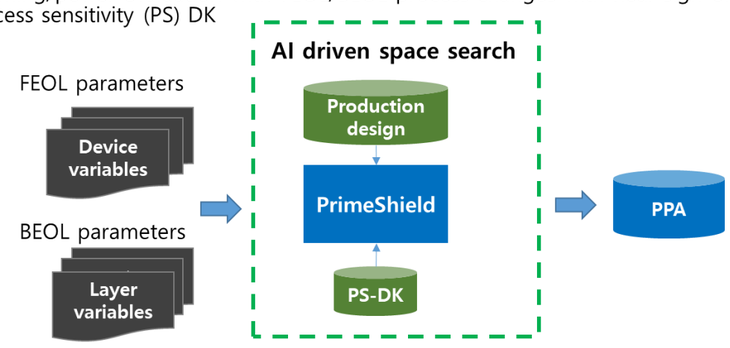
Motivations

- Silicon tuning to find sweet spot for chip performance without changing design
  - Design is already finished, however silicon performance and power are worse than expected target values
  - Revision of design make product costly → process can be tuned by shifting FEOL/BEOL parameters to enhance performance and power
  - Optimal point of silicon target depends on the design → design-process co-optimization is required
  - Silicon experiment to find optimal point is very expensive → not possible to consider all possible combinations of FEOL/BEOL parameters
- Objective
  - Simulation based sweet spot search to enhance frequency and reduce power before silicon experiment
  - Considering both FEOL/BEOL at the same time to find the realistic optimal point
  - AI based approach to get the result within reasonable computing resources

Design-Specific Process Sweet Spot Exploration

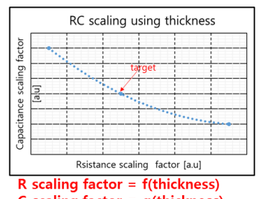
- Evaluate PPA impact by altering FEOL and BEOL process variants
  - Efficient timing/power evaluation with FEOL/BEOL process changes with near sign-off accuracy using process sensitivity (PS) DK



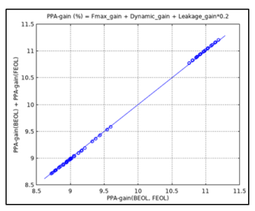
  - Utilize the physical/electrical properties of applications to effectively drive AI optimal search in a huge optimization space
  - Provide a powerful capability to precisely identify PPA Pareto front

FEOL and BEOL Co-optimization to Maximize PPA Gains

- Find optimal FEOL and BEOL process parameters without changing design GDS
  - Baseline design has been PPA optimized
  - FEOL process parameters
    - 6 Vth parameters: {SLVT, LVT, RVT} x {PFET, NFET}
    - Search range: [-30mV, +30mV] with a resolution of 5mV → Search space: 13^6 (4.8M)
  - BEOL process parameters
    - Auto RC scaling using thickness parameter, no RC extraction required
    - 12 metal layers: {M1,M2,M3,M4,M5,M6,M7,M8,M9,M10,M11,M12}
    - Search range: [-20%, +20%] with a resolution of 10% metal thickness → Search space: 5^12 (244M)
  - Co-optimization search space: 4.8M x 244M = 1.17*10^15



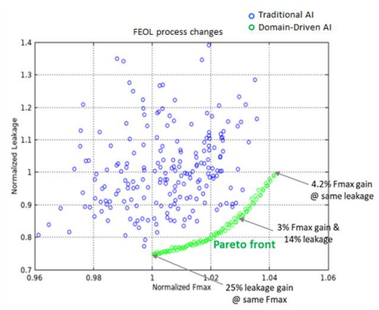
R scaling factor = f(thickness)
C scaling factor = g(thickness)

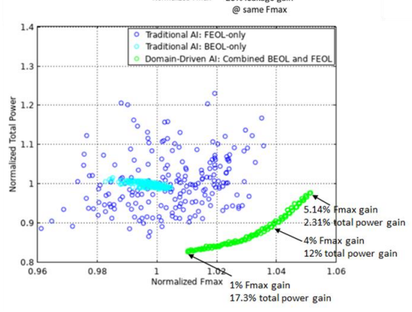


- Proposed FEOL and BEOL co-optimization
  - Observed weak correlation between FEOL and BEOL optimization
    - Select top M FEOL sample and Top N BEOL samples
    - Perform FEOL/BEOL co-optimization to cover M x N search space → significantly reduce search space (M+N)
  - Maximize PPA gains
    - FEOL only: Freq/leakage
    - FEOL/BEOL co-optimization: Freq/leakage/dynamic

Experimental Results

- Design
  - 4nm production CPU, 6M instances
  - 6 Vth parameters and 12 metal layers
  - PPA optimized using existing PDK
- FEOL optimization
  - Domain-driven AI for sweet spot exploration
    - Effectively identify PPA Pareto front with only 100 STA runs
    - TAT: 0.5 day
  - Provide users a capability to select optimal solutions based on actual PPA needs
    - Fmax boost: 4% Fmax gain with the same leakage
    - Leakage boost: 25% leakage gain with the same Fmax
    - Both Fmax and Leakage boost: 3% Fmax gain and 14% leakage gain
- FEOL and BEOL co-optimization
  - Optimal solutions
    - Fmax boost: 5% Fmax gain with 2% total power gain
    - Total power boost: 17% total power reduction with similar 1% Fmax gain
    - Both Fmax and power boost: 4% Fmax gain and 12% power reduction
  - Runtime: 2 days (200 STA runs)





Summary

- We presented a novel approach to perform design-process co-optimization on production designs with reasonable runtime
  - Efficiently assess PPA gain by altering process parameters with near sign-off accuracy
  - Domain-driven AI search to enable powerful PPA sweet spot search and generate PPA pareto front very quickly
  - FEOL and BEOL co-optimization to maximize PPA gains
- For high-volume production chips, the proposed approach can deliver significant PPA benefit on top of conventional approach (process optimized for small test block vs actual production design)
- Very encouraging results based on 4nm production CPU design
  - PPA Pareto front allow users to flexibly select the optimal process based on PPA needs
  - FEOL and BEOL co-optimization can maximize Performance and Power

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